# P2 Threads

There is a potential race hazard in the P2 software with different threads accessing the same register. A solution is needed. One way may be to rearrange resisters so that only one thread needs to access each register.

Each P2 message is sent to a different port number, and handled by a different thread. Look at what data is in what messages.

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| **IP** | **Byte Address** | **Register** |  | **Reference** |
| Config256\_RX\_0 | 0x00000 | DDC0 Frequency |  | High priority. Not shared – no hazard |
| Config256\_RX\_0 | 0x00004 | DDC1 Frequency |  | High priority. Not shared – no hazard |
| Config256\_RX\_0 | 0x00008 | DDC2 Frequency |  | High priority. Not shared – no hazard |
| Config256\_RX\_0 | 0x0000C | DDC3 Frequency |  | High priority. Not shared – no hazard |
| Config256\_RX\_0 | 0x00010 | DDC4 Frequency |  | High priority. Not shared – no hazard |
| Config256\_RX\_0 | 0x00014 | DDC5 Frequency |  | High priority. Not shared – no hazard |
| Config256\_RX\_0 | 0x00018 | DDC6 Frequency |  | High priority. Not shared – no hazard |
| Config256\_RX\_0 | 0x0001C | DDC7 Frequency |  | High priority. Not shared – no hazard |
| Config256\_RX\_1 | 0x01000 | DDC8 Frequency |  | High priority. Not shared – no hazard |
| Config256\_RX\_1 | 0x01004 | DDC9 Frequency |  | High priority. Not shared – no hazard |
| Config256\_RX\_1 | 0x01008 | RX Test DDS Frequency |  | Setup only. Not shared – no hazard |
| Config256\_RX\_1 | 0x0100C | DDC Rate register |  | DDC specific packet (rates). No hazard |
| Config256\_RX\_1 | 0x01010 | DDC Input Select Register |  | DDC specific packet (ADC selection)  Outgoing DDC I/Q (enable)  Hazard exists |
| Config256\_RX\_1 | 0x01014 | Unused |  | n/a |
| Config256\_RX\_1 | 0x01018 | Unused |  | n/a |
| Config256\_RX\_1 | 0x0101C | Unused |  | n/a |
| Config256\_2 | 0x02000 | KeyerConfig |  | Transmitter specific. Setup. No conflict |
| Config256\_2 | 0x02004 | CodecConfig |  | Transmitter specific. Setup. No conflict |
| Config256\_2 | 0x02008 | TXConfig |  | Mostly setup. Transmitter specific enables keyer.  No obvious conflict. |
| Config256\_2 | 0x0200C | TXFrequency |  | High priority. No conflict. |
| Config256\_2 | 0x02010 | TX Modulation test source |  | Setup/debug only. No conflict. |
| Config256\_2 | 0x02014 | RF GPIO | [3:0] mic/ PTT/bias sel  [4] Spkr mute  [13:8] ADC rand/dither  [22:16] open collector  [23] MOX  [27] TX relay disable  [29] ATU tune  [30] xvtr enable | TX specific  High priority  DDC specific  High priority  High Priority  High Priority ?  High Priority  Hazard exists! |
| Config256\_2 | 0x02018 | ADC\_Ctrl |  | High Priority |
| Config256\_2 | 0x0201C | DAC\_Ctrl |  | High Priority |
| ConfigReg\_64\_0 | 0x03000 | Processor LED |  | Not used. |
| ReadReg\_64\_0 | 0x04000 | Status |  | Read only |
| ReadReg\_64\_0 | 0x04004 | Date code Register |  | Read only |
| Axi\_FIFO\_overflow\_0 | 0x05000 | ADC Overflow | ADC1, 2 latched overflow bits | Read only |
| Receiver/ Axi\_FIFO\_overflow\_0 | 0x06000 | FIFO Overflow | DDC mux input FIFO overflow bits | Read only (but with side effect) |
| ConfigReg\_64\_0 | 0x07000 | FIFO Clear | DDC, DUC, Mic & Spk FIFO reset bits | Shared. Hazard exists. |
| Fifo\_Monitor\_0 | 0x09000 | FIFO monitor | RX DDC FIFO, TX DUC FIFO, Codec RX FIFO, Codex TX FIFO | Read only in use |
| AXI\_SPI\_ADC\_0 | 0x0A000 | SPI ADC reader | Alex analogue inputs | Read only |
| Axilite\_Alex\_SPI\_0 | 0x0B000 | AXILite\_Alex\_SPI | SPI interface to RF board | High priority |
| ReadReg\_64\_ID | 0x0C000 | ID1 | Version ID (31:16)  Revision (15:4)  Clock monitor bits(3:0) | Read only |
| ReadReg64\_ID | 0x0C004 | ID2 | Product ID (31:16)  S/W ID (15:0) | Read only |
| Axi\_quad\_spi\_0 | 0x10000 | SPI Config Prom | Xilinx SPI interface | Not used by p2app |
| Axil\_SPIWriter\_0 | 0x14000 | SPI codec bus | Codec registers | TX specific |
| Axadwiz\_0 | 0x18000 | On-chip XADC | Xilinx XADC interface | Not used. Read only. |
| Axi\_BRAM\_ctrl\_0 | 0x1C000 | AXI block RAM access | CW keyer ramp waveform | Setup only. |